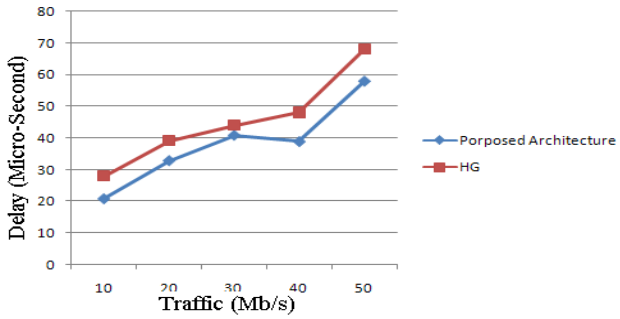

Fig.12. Delay in exponential traffic model

VII. Conclusion

The mesh on chip is a new outlook for solving the problems of flexibility, scalability and reliability in various applications. The efficiency of mesh on chip depends mainly on the techniques of routing being used. In this paper a new designation is suggested in which fewer switches and connections are in comparison to previous designations. By using this method, the cost of implementation decreases to a reasonable level.

Furthermore in the architecture recommended here, maximum steps required for a packet to travel between the origin and destination have been reduced with respect to mesh architecture; by means of increasing the efficiency.

Finally, doing some alterations in hierarchical graph architecture improves its performance. All methods suggested in this paper are simulated by NS2 software.

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